What is claimed is

1. A matrix array substrate comprising:

scanning lines arranged substantially in parallel;

signal lines arranged substantially perpendicular to the scanning lines;

pixel electrodes each being arranged on a respective patch in a matrix formed by the scanning and signal lines;

each switching element being disposed at around intersection of one of the scanning lines and one of the signal lines and inputting signal to respective one of the pixel electrodes from said one of signal lines in accordance with electric current on said one of scanning lines;

a storage-capacity-forming extended portion being extended from first of the pixel electrode towards second of the pixel electrode, said first pixel electrode being interposed between first and second ones of the scanning lines and being supplied with a signal in accordance with an applied current on the first scanning line, said second pixel electrode being supplied with a signal in accordance with an applied current on the second scanning line, and said storage-capacity-forming extended portion overlapping the second scanning line with an insulator film therebetween; and

a tandem repair circuit;

said tandem repair being comprised of;

first connector electrode being connected with the storage-capacity-forming extended portion extended from the first pixel electrode;

second connector electrode being distanced from the first connector electrode and connected with said second pixel electrode;

third connector electrode disposed as bridging over the first connector electrode to the second connector electrode; and

a contact hole passing through an insulator film, for electrically connecting the first connector electrode to the storage-capacity-forming extended portion, said contact hole being placed within contours of said second scanning line.

2. A matrix array substrate according to claim 1,

said first connector electrode being comprised of;

a thin-width wiring portion extending from an area above said third connector electrode to an area above said one of scanning line and substantially perpendicularly crossing a contour of said one of scanning lines; and

a thick-width wiring portion being connected with an end of said thin-width wiring portion and located within contours of said scanning lines.

3. A matrix array substrate according to claim 1, said

thick-width wiring portion having a size along the scanning line larger than width of the scanning line.

4. A matrix array substrate according to claim 1, wherein said size of the thick-width wiring portion is substantially equal with a sum of a size of said contact hole and a margin for absorbing deviation of alignment during patterning of said contact hole.

5. A matrix array substrate according to claim 1,

said each switching element being comprised of; a gate electrode formed of said first scanning line or a portion extended therefrom; a drain electrode formed of said first signal line or a portion extended therefrom; and a source electrode connected with said first pixel electrode through a contact hole passing through the insulator film; and

said second connector electrode being formed of a portion extended from said source electrode.

6. A matrix array substrate according to claim 1,

said third connector electrode being included in a first-layer metal pattern and formed simultaneously with the scanning lines, and said first and second connector electrodes being included in a second-layer metal pattern and formed simultaneously with the signal lines.

7. A matrix array substrate according to claim 6, said second-layer metal pattern being formed of aluminum metal or its alloy.

8. A matrix array substrate according to claim 1, wherein said pixel electrodes and said storage-capacity-forming extended portions are included in a pattern of transparent electric-conductive material, which is disposed in a layer above said first- and second-layer metal pattern.

9. A matrix array substrate comprising:

a first-layer wiring pattern including scanning lines and gate electrodes arranged on an insulator substrate; a gate insulator film covering the first-layer wiring pattern; a second-layer wiring pattern including signal lines and source and drain electrodes; light reflective pixel electrodes each being connected with respective one of the source electrodes; and

a storage-capacity-forming extended portion being extended from first of the pixel electrode towards second of the pixel electrode, said first pixel electrode being interposed between first and second ones of the scanning lines and being supplied with a signal in accordance with an applied current on the first scanning line, said second pixel electrode being

supplied with a signal in accordance with an applied current on the second scanning line, and said storage-capacity-forming extended portion overlapping the second scanning line with an insulator film therebetween;

further comprising:

an island pattern being included in said second-layer wiring pattern and disposed within an overlapping area in which said storage-capacity-forming extended portion overlaps said second scanning line, and said island pattern having a size along said second scanning line larger than width of said second scanning line.

10. A matrix array substrate according to claim 9, further comprising a contact hole on an insulator film covering the island pattern, for electrically connecting with said storage-capacity-forming extended portion.

11. A matrix array substrate according to claim 10, wherein said size of the t island pattern is substantially equal with a sum of a size of said contact hole and a margin for absorbing deviation of alignment during patterning of said contact hole.